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10/764,095	01/23/2004	Douglas Durham	15436.163.1	8239

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EXAMINER	
PASIA, REDENTOR M	
ART UNIT	**PAPER NUMBER**
2474	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/764,095	DURHAM ET AL.	
	Examiner	Art Unit	
	REDENTOR M. PASIA	2474	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) *2,6-14,18 and 20-40* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,15-17 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

*****Please note change of AU 2416 to AU 2474*****

Response to Amendment

1. Applicant's amendment filed on 07/13/2009 has been entered. Claims 1, 4, 15 and 19 have been amended. No claims have been added or cancelled. Claims 1-40 are still pending in this application, of which, claims 2, 6-14, 18, and 20-40 are withdrawn from consideration, and with claims 1 and 15, being independent.

Response to Arguments

2. Applicant's arguments, see Applicant's Remarks, filed 07/13/2009, with respect to claims 1, 3-5, 15-17 and 19 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claim 5** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. **Claim 5** recites the limitation "the reference clock" in lines 1-2. It is not clear if the limitation "the reference clock" in lines 1-2 refers to "the reference clock frequency" in line 13 of claim 1. If they are related, the limitation "the reference clock" in line 1-2 must be revised to "the reference clock frequency" If they are not related, the limitation "the reference clock" must be revised to "[[the]] a reference clock". There is insufficient antecedent basis for this limitation in the claim.

6. However in the examination of the claims, the Examiner has interpreted the limitation "the reference clock in lines 1-2 as being related to "the reference clock frequency" in line 13 of claim 1.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. **Claims 1, 3-5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chamdani et al. (US 7,133,416; hereinafter Chamdani) in view of Yu et al. (US 6,070,248; hereinafter Yu).

As to claim 1, Chamdani shows a method (Figure 1 shows system 50 which performs at least the methods in Figures 13 and 16) defining a common time base (Figure 16; note clock recovery and setting of clock frequency based on communication protocol) suitable for use in connection with the operation of a multi-link protocol analyzer (Figure 1, system 50; note that system 50 process packets of different communications protocols as shown in Figures 4-5; also, system 50 also performs clock recovery from different protocols and setting of clock frequency based on received protocol. Thus, the Examiner views system 50 functioning as a multi-link protocol analyzer) in a multi-protocol communications system (Figure 1; note system 10 includes multiple protocols including Fiber Channel (FC), Infiniband (IB), and Gigabit Ethernet (GE).), the method comprising:

determining a first protocol clock frequency (Figure 13 and 16; clock recovery is performed to determine the clock frequency at which the data packets of a particular/first protocol operates) at a first link analyzer of the multi-link protocol analyzer (Figure 2 shows system 50 (i.e. multi-link protocol analyzer); Figure 14 shows system 800 (i.e. first link analyzer) including interface converter paddle 70, physical layer card 72 and line card board 54, wherein system 800 is dedicated to a particular communication protocol (i.e. IB, FC or GE).),

the first protocol clock frequency being associated with a first communications protocol associated with the multi- protocol communications system (Figures 1-2, 13-14 and 16; note that data packets received at interface converter paddle 70 of system 50 is associated with a

communication protocol (i.e. FC being first protocol having a corresponding protocol clock frequency).);

determining a second protocol clock frequency (Figure 13 and 16; clock recovery is performed to determine the clock frequency at which the data packets of a second protocol operates; it should be further noted that the methods of Figure 13 and 16 are performed at each system 800 in Figure 14; Figure 2 shows a plurality of combination corresponding to system 800 in Figure 14) at a second link analyzer of the multi-link protocol analyzer (Figure 2 shows system 50 (i.e. multi-link protocol analyzer); another combination of system 800 in figure 2 (i.e. second link analyzer) including interface converter paddle 70, physical layer card 72 and line card board 54, wherein system 800 is dedicated to a particular communication protocol (i.e. IB, FC or GE).),

the second protocol clock frequency being associated with a second communications protocol associated with the multi-protocol communications system (Figures 1-2, 13-14 and 16; note that data packets received at interface converter paddle 70 of system 50 is associated with a communication protocol (i.e. IB being the second protocol having a corresponding protocol clock frequency).);

wherein the second protocol clock frequency is unrelated to the first protocol clock frequency (Figure 1, shows multiple communications protocols (i.e. IB, FC or GE); each having a different clock frequency as determined in Figures 13 and 16).

Chamdani shows all the elements, including the first and second protocol clock frequencies. However, Chamdani does not specifically show a step of using first and second

clock frequencies as a basis for determining a reference clock frequency, where the reference clock frequency is different from each of the first and second clock frequencies.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Yu. Yu shows a clock signal generator within an electronic device locally generates a reference clock signal having a reference frequency from a base clock signal having a base frequency (abstract; Figure1).

Specifically, Yu shows the step of using first and second clock frequencies as a basis for determining a reference clock frequency (Figures 1-4; col. 1, line 66 to col. 2, line 8; col. 3, lines 12-54; note reference clock is generated based on the base clock signal; also note that the reference clock varies depending on the base clock signal source present in any of the plurality of computers. Thus it can be seen, the reference clock is based on the base clock frequencies supplied by the computers.),

where the reference clock frequency is different from each of the first and second clock frequencies (Figure 3-4; col. 3, lines 49-58; note reference clock can either have the value of 1 MHz or 10 MHz, while base clock frequencies have values of 2.5 MHz, 20 MHz, 25 MHz, or 33 MHz.).

In view of the above, having the system of Chamdani, then given the well-established teaching of Yu, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Chamdani as taught by Yu, in order to allow generation of a reference clock signal having a stable reference frequency even when the base frequency of the base clock may vary (col. 2, lines 6-9).

As to claim 3, modified Chamdani shows all of the elements including the first and second protocol clock frequencies, except for the step of selecting the reference clock frequency to be higher than the first and second clock frequency.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Yu. Specifically, Yu shows the step of selecting the reference clock frequency to be higher than the first and second clock frequency (Figure 3-4; col. 3, line 40-60; col. 4, lines 13-49; note that the reference frequency can have a value of 10MHz, while the base frequency can have a value of 2.5 MHz.).

In view of the above, having the system of modified Chamdani, then given the well-established teaching of Yu, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of modified Chamdani as taught by Yu, in order to allow generation of a reference clock signal having a stable reference frequency even when the base frequency of the base clock may vary (col. 2, lines 6-9).

As to claim 4, modified Chamdani shows wherein the first and second communications protocols include *at least one of* the following communications protocols: Infiniband (Chamdani: Figure 1, Infiniband (IB).); Gigabit Ethernet (Chamdani: Figure 1, Gigabit Ethernet (GE).); SONET; Fibre Channel (Chamdani: Figure 1; Fiber Channel (FC).); and, PCI Express.

As to claim 5, modified Chamdani shows all of the elements including the reference clock and multi-protocol communications system, except for using the reference clock as a basis to determine at least one of the following: a relative chronological order of selected data events concerning a communications system; and, relative timing of selected data events concerning a communications system.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Yu. Specifically, Yu shows using the reference clock as a basis to determine *at least one* of the following:

a relative chronological order of selected data events concerning the multi-protocol communications system; and

relative timing of selected data events concerning a communications system (col. 2, lines 29-37; note that the present invention may be used to generate a reference clock signals for timing events within an Ethernet computer network peripheral device coupled between a computer host system and a computer network; the base signal source may be from the computer host system or the computer network, and the storage device containing the value of the base frequency may be an EEPROM within the computer host system or the computer network.)

In view of the above, having the system of modified Chamdani, then given the well-established teaching of Yu, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of modified Chamdani as taught by Yu, in order to allow generation of a reference clock signal having a stable reference frequency even when the base frequency of the base clock may vary (col. 2, lines 6-9).

10. **Claims 15-17 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chamdani et al. (US 7,133,416; hereinafter Chamdani) in view of Strong et al. (US 6,335,931; hereinafter Strong) in view of Yu et al. (US 6,070,248; hereinafter Yu).

As to claim 15, Chamdani shows a protocol analyzer (Figure 1 shows system 50 which performs at least the methods in Figures 13 and 16; further note that system 50 processes packets

of different communications protocols as shown in Figures 4-5; also, system 50 also performs clock recovery from different protocols and setting of clock frequency based on received protocol. Thus, the Examiner views system 50 functioning as a multi-link protocol analyzer)

configured for use in connection with processing data events (Figure 13 and 16; note system 50 process packets where the processing includes reception of data packets, clock recovery of a particular protocol related to the received data packet and transmission of data packets) associated with a multi-protocol communications system (Figure 1; note system 10 includes multiple protocols including Fiber Channel (FC), Infiniband (IB), and Gigabit Ethernet (GE).), the protocol analyzer comprising:

a first link analyzer (Figure 2 shows system 50 (i.e. multi-link protocol analyzer); Figure 14 shows system 800 (i.e. first link analyzer) including interface converter paddle 70, physical layer card 72 and line card board 54, wherein system 800 is dedicated to a particular communication protocol (i.e. IB, FC or GE).)

configured to receive data (Figure 13 and 16; note reception of data packets) from a first communication link (Figure 2, 13, and 16; note link 60)

wherein the first link is associated with a first protocol clock frequency (Figure 1-2, 14; note link 60 receives data packets related to different protocols (i.e. IB, FC, or GE); Figure 14 shows system 800 (i.e. first link analyzer) including interface converter paddle 70, physical layer card 72 and line card board 54, wherein system 800 is dedicated to a particular/first communication protocol.),

the first protocol clock frequency being associated with a first communication protocol (Figures 1-2, 13-14 and 16; note that data packets received at interface converter paddle 70 of

system 50 is associated with a communication protocol (i.e. FC being first protocol having a corresponding protocol clock frequency).); and

a second link analyzer (Figure 2 shows system 50 (i.e. multi-link protocol analyzer); another combination of system 800 in figure 2 (i.e. second link analyzer) including interface converter paddle 70, physical layer card 72 and line card board 54, wherein system 800 is dedicated to a particular communication protocol (i.e. IB, FC or GE).)

in at least indirect communication with the first link analyzer (Figure 1-2; note that each combination of system 800 are part of the over-all system 50 and thus, seen as having indirect communication with the other system 800 in system 50) and

configured to receive data from a second communication link (Figure 13-14 and 16; it should be further noted that the methods of Figure 13 and 16 are performed at each system 800 in Figure 14; Figure 2 shows a plurality of combination corresponding to system 800 in Figure 14),

wherein the second link is associated with a second protocol clock frequency (Figure 1-2, 14; note link 60 receives data packets related to different protocols (i.e. IB, FC, or GE); Figure 2 shows the plurality of system 800 (i.e. second link analyzer) including interface converter paddle 70, physical layer card 72 and line card board 54, wherein system 800 is dedicated to a second communication protocol.),

the second protocol clock frequency being associated with a second communication protocol (Figures 1-2, 13-14 and 16; note that data packets received at interface converter paddle 70 of system 50 is associated with a communication protocol (i.e. IB being the second protocol having a corresponding protocol clock frequency).),

the second protocol clock frequency being unrelated to the first protocol clock frequency (Figure 1, shows multiple communications protocols (i.e. IB, FC or GE); each having a different clock frequency as determined in Figures 13 and 16).

It is noted that the system of Chamdani shows the processing of packets including a process of clock recovery (Figure 16).

Even though, Chamdani shows all of the elements, Chamdani does not show wherein each of the first and second link analyzers are also being configured to receive and transmit a trigger and a reference clock, and each of the first and second link analyzers are further configured to timestamp data in association with the reference clock, wherein the reference clock is determined by the first and second protocol clock frequencies, the reference clock being different from each of the first and second protocol clock frequencies.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Strong. Specifically, Strong shows wherein each of the first and second link analyzers (Figure 1, network analyzer 100 and 101) also being configured to receive and transmit a trigger (Figure 1; note trigger in 128a, 128b and trigger out 126a, 126b used by each network analyzer device to perform trigger operations) and a reference clock (Figure 2, clock in 222a, 222b and clock out 220a, 220b used by each network analyzer device to perform clock synchronization; col. 2, lines 55-61; col. 5, lines 12-48; same clock source.), and

each of the first and second link analyzers are further configured to timestamp data in association with the reference clock (Figure 1-2; col. 2, lines 55-61; col. 5, lines 12-48; note that the network analyzer device timestamps data packets since they are derived from the same clock source.).

In view of the above, having the system of Chamdani, then given the well-established teaching of Strong, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Chamdani as taught by Strong, in order to synchronize clocks on devices in a network so that time stamps placed on data packets transmitted into and collected from multiple segments on that network are synchronized with respect to each other (col. 2, lines 35-43).

Still, modified Chamdani does not show the reference clock is determined by the first and second clock frequencies, the reference clock being different from each of the first and second clock frequencies.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Yu. Yu shows a clock signal generator within an electronic device locally generates a reference clock signal having a reference frequency from a base clock signal having a base frequency (abstract; Figure1).

Specifically, Yu shows the reference clock is determined by the first and second clock frequencies (Figures 1-4; col. 1, line 66 to col. 2, line 8; col. 3, lines 12-54; note reference clock is generated based on the base clock signal; also note that the reference clock varies depending on the base clock signal source present in any of the plurality of computers. Thus it can be seen, the reference clock is based on the base clock frequencies supplied by the computers given in the network),

the reference clock being different from each of the first and second clock frequencies (Figure 3-4; col. 3, lines 49-58; note reference clock can either have the value of 1 MHz or 10 MHz, while base clock frequencies have values of 2.5 MHz, 20 MHz, 25 MHz, or 33 MHz.)..

In view of the above, having the system of modified Chamdani, then given the well-established teaching of Yu, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of modified Chamdani as taught by Yu, in order to allow generation of a reference clock signal having a stable reference frequency even when the base frequency of the base clock may vary (col. 2, lines 6-9).

As to claim 16, modified Chamdani shows wherein at least one of the link analyzers is configured to generate the reference clock (Chamdani: Figure 2, 14, and 16; note one of system 800 in Figure 2; Figure 16 shows clock frequency is set according to communication protocol. Since the clock frequency is set to a new value, the resultant can be seen as a generated clock frequency).

As to claim 17, modified Chamdani shows at least one of the link analyzers is configured to generate the trigger (Strong: Figures 1-2; col. 4, line 57 to col. 5, lines 10; note that either network analyzer device 100 or 101 can act as the generator of the trigger operations).

As to claim 19, modified Chamdani shows all of the elements including the first and second protocol clock frequencies, except wherein the reference clock has a frequency that is higher than the first and second clock frequency.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Yu. Specifically, Yu shows wherein the reference clock has a frequency that is higher than the first and second clock frequency (Figure 3-4; col. 3, line 40-60; col. 4, lines 13-49; note that the reference frequency can have a value of 10MHz, while the base frequency can have a value of 2.5 MHz.).

In view of the above, having the system of modified Chamdani, then given the well-established teaching of Yu, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of modified Chamdani as taught by Yu, in order to allow generation of a reference clock signal having a stable reference frequency even when the base frequency of the base clock may vary (col. 2, lines 6-9).

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to REDENTOR M. PASIA whose telephone number is (571)272-9745. The examiner can normally be reached on M-F 7:00am to 3:30pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Aung Moe can be reached on (571)272-7314. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aung S. Moe/
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